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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/054,358	01/17/2002	Chinnugounder Senthilkumar	10559/650001/P12972	5789

20985 7590 04/23/2003

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EXAMINER
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ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 04/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
10-054,358	Senthikumar et al.
Examiner	**Group Art Unit**
SHINGLETON	2817

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

P riod for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE Three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-27 is/are pending in the application.

Of the above claim(s) 19-23 is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-18, 24-27 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement

Application Papers

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).

☐ All ☐ Some* ☐ None of the:

☐ Certified copies of the priority documents have been received.

☐ Certified copies of the priority documents have been received in Application No. _____.

☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: _____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☒ Notice of Reference(s) Cited, PTO-892 3 Sheets

☐ Notice of Draftsperson's Pat nt Drawing R view, PTO-948

☐ Int rview Summary, PTO-413

☐ Notice of Informal Pat nt Application, PTO-152

☐ Other _____

Office Action Summary

DETAILED ACTION

Election/Restrictions

I. Claims 1-18 and 24-27, drawn to an oscillator arrangement, classified in class 331, subclass 36C.

II. Claims 21-23 drawn to a variable capacitor element, classified in class 361, subclass 271.

III. Claims 19 and 20 drawn to a calibration system, classified in class 73, subclass 1.43.

Inventions I and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the combination does not require the independent control signal generated by a logic circuit and the buffer circuitry that decouples the capacitors from the logic circuit. The subcombination has separate utility such as for use in filter circuits.

Inventions III and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the combination does not recite the variable capacitance features or the independent control signal generated by a logic circuit and the buffer circuitry that decouples the capacitors from the logic circuit. The subcombination has separate utility such as for use in filter circuits.

Inventions III and I are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the combination does not require the specific details of the oscillator, namely the independently selectable capacitors or the digitally tunable oscillator. The subcombination has separate utility such as an oscillator used in non-network device such as a waveform generator.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conservation with Mr. Rex Wong on April 14, 2003 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-18 and 24-27 directed toward an oscillator arrangement. Affirmation of this election must be made by applicant in replying to this Office action. Claims 19-23 have been withdrawn from further consideration by the examiner. 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 13, 16, 24, 26 and 27 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Clarke US 6,337,604 (Clarke).

The single Figure of Clarke discloses a circuitry for controlling the oscillating frequency of an oscillator (See column 2, line 22), the circuitry having a plurality of on-chip capacitors C1-C6, each of which is independently selectable by a control signal D_0-D_5, and each of which provides a controllable amount of capacitance to the oscillator to control the oscillating frequency of the oscillator (See column 2, line 22).

The single Figure of Clarke also discloses an electronic device comprising a real time clock, i.e. oscillator, for generating a system time signal "CLK OUT 5" (See the only Figure and column 2, around line 20), the real ~~time~~ clock having a digitally tunable oscillator (Note the use of set of shift registers 21) for digitally adjusting an operating frequency of the real time clock to speed up or slow down the system time signal (See column 3, lines 45), and a memory device 21 for storing data representing a configuration of the digitally adjusted tunable oscillator.

As it relates to at least claim 16, Clarke also discloses a method for generating a set of control signals D_0-D_5 to select a subset of capacitors from a set of capacitors C1-C6, connecting the selected subset of capacitors to an oscillator 1, generating an oscillating signal using the oscillator and the selected subset of capacitors in combination, and generating a system time signal CLK OUT 5 (See the only Figure in Clarke.) using the oscillating signal.

As it relates to at least claim 24 the only figure of Clarke clearly illustrates an apparatus having a control unit 7, 23, 21 configured to generate a set of control signals D_0-D_5 , each of which independently selects a capacitor from a plurality of capacitors, the selected capacitors being coupled to an oscillator 1, the selected capacitors in combination proving a controllable amount of capacitance to the oscillator to control the oscillating frequency of the oscillator (See column 2, line 22). As it clearly apparent from the only Figure of Clarke the system time signal CLK OUT 5 shown in the only Figure is based upon the

oscillating frequency of the oscillator. The data processing unit 23 processes the data based on the system time signal that is applied to the element 7 of Clarke and the register stores the configuration of the set of control signals as are both clearly apparent from the only Figure in Clarke.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-6, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke US 6,337,604 (Clarke)

All the same reasoning as applied in the 35 USC 102 rejection of claims 1, 13, 16, 24, 26 and 27 and the following: Clarke is silent on the composition of the capacitors C1-C6 and the values of these capacitors. Claims 3-6 merely recites conventional forms of capacitors that make up the frequency changing capacitors of the oscillator.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted any of the conventional capacitors as recited by the claims of the instant application in place of the generic capacitors of Clarke because, as the reference is silent as to the exact composition of the capacitors, any art-recognized equivalent capacitors would have been usable such as the well-known capacitors as recited by the claims of the instant application.

As it relates to claim 2, selection of the frequency changing capacitors to be different from each other is merely the selection of the optimum or workable range. This involves but routine skill in the art and accordingly it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the capacitance values to be any value within the optimum or workable range so as to shift the frequency in a controllable predetermined stepwise manner.

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke US 6,337,604 (Clarke) in view of Kuhn Jr. US 3,930,169 (Kuhn, Jr.).

All the same reasoning as applied in the 35 USC 102 rejection of claims 1, 13, 16, 24, 26 and 27 and the following: Clarke is silent on the composition of the switches 9-19(a,b) that switches the capacitors in and out of the circuit so as to change the frequency of the oscillator.

Transmission gate switches are conventional switching means as noted by Kuhn, Jr. (See Figure 1 and column 4, lines 3-29).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted conventional transmission gate switches in place of the generic switches of Clarke because, as the reference is silent as the exact switching element employed, any art-recognized equivalent switch would have been usable such as the well-known, conventional transmission gate switch as taught by Kuhn, Jr..

As it relates to claim 8, the circuit of Clarke has a "set of registers" 21 to provide the control signals D_0-D_5 for selecting the individual capacitors C1-C6.

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke and Kuhn, Jr. as applied to claims 7 and 8 above, and further in view of Horn "Basic Electronics Theory" 4th Edition pp 377-378 and pp 454-465.

As it relates to claim 9, Clarke is silent on using buffer circuitry to decouple the transmission gate switches from the set of memory registers.

Horn teaches that buffers are used to ensure that the output drive is sufficient to drive the devices on the output thereof.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a buffers between the transmission gate switches and the memory registers so as to insure that there is sufficient drive for the transmission gate switches as taught by Horn.

As it relates to claim 10, Clarke is likewise silent on the use of filtered power signals to power the buffer circuitry. Buffer circuitry requires a power supply as is well known in the art so that it can provide the sufficient drive as noted above. Horn teaches that it is commonplace to utilize filtered power supplies, in particular note pages 456 and 460 to power electronic devices. This as Horn recognizes reduces "ripple", i.e. noise, or voltage fluctuations that then in turn causes less vacillations in the devices powered by such power supplies.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a filtered power supply to power the buffers made obvious above so as to reduce the introduction of noise in the system as is taught by Horn.

Claims 11 and 12 are rejected over Clarke US 6,337,604 (Clarke) in view of Leduc et al. US 6,400,231 (Leduc)

All the same reasoning as applied in the 35 USC 102 rejection of claims 1, 13, 16, 24, 26 and 27 and the following: As it relates to claim 11, Clarke is silent on the use of an inverting amplifier as the element that provides the gain in the oscillator. Clarke utilizes the well-known differential amplifier circuit to provide gain in a crystal oscillator. However, Leduc utilizes an inverting amplifier to provide gain for the oscillator (See column 2, lines 61-62), which is an art recognized equivalent well-known way to provide gain for a crystal oscillator.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the well known differential gain arrangement of Clarke with an inverting amplifier arrangement as these are art recognized equivalent ways to provide gain to a crystal oscillator as taught by Leduc.

As it relates to claim 12, note that the single Figure of Clarke clearly shows the plurality of frequency changing capacitors as being composed of a first subset of the plurality of capacitors that is selectively electrically coupled to a first terminal of the resonator 1, and a second subset of the plurality of capacitors that is selectively electrically coupled to a second terminal of the resonator.

Claims 14, 17 and 18 are Clarke US 6,337,604 (Clarke) in view of Theus et al. US 5,805,029 (Theus).

All the same reasoning as applied in the 35 USC 102 rejection of claims 1, 13, 16, 24, 26 and 27 and the following: Clarke describes in generic terms element 7 as comparing the system time signal CLK OUT 5 to be within a certain frequency range. Clarke, however, is silent on the specifics of such a structure. Note that Clarke saves the data representing the setting of the control signals in memory device 21.

Figure 4 of Theus discloses specific conventional means to compare the system time signal to the reference time signal so that a control signal can be generated to the controller of an oscillator circuit that utilizes the switching of capacitors to change the oscillator frequency. Specifically, Theus discloses receiving a reference time signal 8a and comparing this reference time signal to the system time signal 2a via a comparator 7. This controls which subsets of capacitors C11, C21, C1n, C2n that are connected to the oscillator.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the conventional means of Theus to compare the reference time signal to a system time signal so as to control generate the control signal because, as the Clarke reference is silent on the specific structure of the comparison arrangement 7, any art-recognized equivalent frequency control means would have been usable such as the well-known conventional arrangement of Theus.

Claim 25 is rejected under 35 USC 103 as being obvious over Horn "Basic Electronics Theory" pp 418-426 (Horn) in view of Clarke US 6,337,604 (Clarke).

Horn discloses that as part of the chip-set of a computer system a clock oscillator is included therein (See page 425). Horn however is silent on the exact structure of the computer system clock thus any conventional structure can be used.

The only Figure of Clarke clearly illustrates an conventional clock apparatus having a control unit 7, 23, 21 configured to generate a set of control signals D_0-D_5 , each of which independently selects a capacitor from a plurality of capacitors, the selected capacitors being coupled to an oscillator 1, the selected capacitors in combination proving a controllable amount of capacitance to the oscillator to control the oscillating frequency of the oscillator (See column 2, line 22). As it clearly apparent from the only Figure of Clarke the system time signal CLK OUT 5 shown in the only Figure is based upon the oscillating frequency of the oscillator. The data processing unit 23 process data based on the system time signal that is applied to the element 7 of Clarke and the register stores the configuration of the set of control signals as are both clearly apparent from the only Figure in Clarke.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention to have substituted the conventional clock apparatus of Clarke in place of the generic clock apparatus of Horn because, as the reference is silent as to the exact structure of the clock, any art-recognized material would have been usable such as the well-known conventional clock apparatus of Clarke.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tsumura US 5,977,839 discloses the use of a latch circuit just after the memory circuit so as to apply the output of the memory and hold the output of the memory circuit 3 until instructed otherwise. Koshihisa JP1190106 discloses an oscillator structure that has a transmission gate arrangement (See Figure 6). Williamson US 6,094,105 discloses the use of variable capacitors 5 to shift the frequency of an

oscillator (See Figure 2). Kallio et al. EP 1,134,921 discloses the use of a reference signal from the network to control the clock rate. Note column 5. The following references describe various ways to synchronize clocks: Levine "Time Syncronization over the Internet Using an Adaptive Frequency-Locked Loop", Fasbender et al. "On assessing Unidirectional Latencies in Packet-Switched Networks", Levine "Time Synchronization Using the Internet", Monington et al. "Time Synchronization Using the Internet", Mills "Improved Algorithms for Synchronizing Computer Network Clocks", Lombardi "Computer Time Synchronization", NIST internet time service "Set your computer clock via the Internet", Dallas Maxium Corp. "Evaluating the Accuracy of Maxium Real-Time Clocks (RTCs)", Levine "An Algorithm to Synchronize the Time of a Computer to Universal Time" and Levine "Time Synchronization over the Internet using "Autolock"".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is 703-308-4903. The examiner can normally be reached on Monday-Thursday from 8:00 to 4:30. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (703) 308-4909. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

MBS
April 18, 2003

MICHAEL B SHINGLETON
PRIMARY EXAMINER
GROUP ART UNIT 2817